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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,638	10/31/2003	Dennis D. Tran	P16885	5387
7590	02/13/2006		EXAMINER [REDACTED]	KRAVETS, LEONID
Patrick J Buckley Buckley Maschoff Talwalkar & Allison LLC Five Elm Street New Canaan, CT 06840			ART UNIT [REDACTED]	PAPER NUMBER 2189

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/699,638	TRAN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 27 December 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-22 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 31 October 2003 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

***DETAILED ACTION***

***Response to Amendment***

1. This Office Action has been issued in response to amendment filed 29 November 2005. Claims 1-24 are pending. Applicant's arguments have been carefully and fully considered in light of the instant amendment. Applicant's amendment necessitates a new rejection. Accordingly this action has been made **FINAL**.

***Specification***

2. The previous objection to the specification is withdrawn due to amendment filed December 27, 2005.

***Claim Rejections - 35 USC § 112***

3. The previous rejection under 35 USC 112 is withdrawn due to amendment filed December 27, 2005.

***Claim Rejections - 35 USC § 101***

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 17 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The programming statements are adapted to be translated into code, thus they are not code and are not functional. Storing the statements on a storage medium does not make the statements statutory.

***Claim Rejections - 35 USC § 102***

4. The previous rejection under 35 USC 102 has been withdrawn due to amendment filed December 27, 2005.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-9 and 14-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakhimovsky (US Patent 6,058,460) and further in view of Rishi (US Patent 5,953,530).

As per claim 1, Nakhimovsky discloses a method, comprising:

Determining retrieving a set of programming statements associated with a multithreaded network processing element, the network processing element having a local memory [The method of Nakhimovsky describes a processing element having an associated memory pool in the system memory; wherein the method is applicable to any application requiring parallel memory management. A network processing element is interpreted to be a processor having parallel threads requiring memory management (Col 1, Lines 47-52, 61-62)];

arranging for a first portion of the local memory to be allocated to a first thread context (Col 3, Lines 1-4) in accordance with a programming statement that is associated with a first thread and symbolically references a buffer name [Nakhimovsky

discloses memory pools being numbered, since each memory pool contains a buffer, the buffers are also numbered (Col 5, Lines 54-55)]. Nakhimovsky does not disclose that the programming statement includes an indication of a read/write status of the first portion. Rishi discloses a library routine allocating memory space to threads having a read/write status (Col 13 Lines 48-55; Col 14, Lines 1-11); and

arranging for a second portion of the local memory to be allocated to a second thread context (Col 3, Lines 1-4) in accordance with a programming statement that is associated with a second thread and symbolically references the buffer name [Nakhimovsky discloses memory pools being numbered, since each memory pool contains a buffer, the buffers are also numbered (Col 5, Lines 54-55)]. Nakhimovsky does not disclose that the programming statement includes an indication of a read/write status of the first portion. Rishi discloses a library routine allocating memory space to threads having a read/write status (Col 13 Lines 48-55; Col 14, Lines 1-11); and

wherein the symbolically referenced buffer name includes both letters and numbers [It would be obvious to use a name having both letters and numbers instead of just numbers to make identification of a thread easier. Furthermore, using numbers of Nakhimovsky is equivalent to the claimed letters and numbers since the computer system converts all letters and numbers to binary code, thus the representation is equivalent].

As per claim 2, Nakhimovsky and Rishi disclose the method of claim 1, Rishi further discloses the method comprising: including a base, size, and offset with the

programming statement associated with the first thread [The disclosed library routine includes stack size, stack base address and thread pointer. Note that Rishi discloses a thread pointer instead of an offset, these are interpreted to be equivalent, since a pointer offsets to the necessary location. Further, the library routine contains programming statements associated with each thread allocation of malloc (Col 14; Lines 41-54; Col 15, Lines 7-47)].

~~wherein said determining comprises retrieving the set of programming statements from a storage device.~~

As per claim 3, Nakhimovsky discloses the method of claim 1, wherein said arranging comprises translating the programming statements into code [Programming statements must be translated into code for them to be understood by a computer, and therefore, to arrange the memory of claim 1 (Col 2, Line 67 – Col 3, Line 2)].

As per claim 4, Nakhimovsky and Rishi disclose the method of claim 1, Nakhimovsky further discloses the method comprising:

arranging for information associated with the first thread context to be stored in the first portion of the local memory (Col 4, Lines 3-8); and  
arranging for information associated with the second thread context to be stored in the second portion of the local memory (Col 4, Lines 3-8).

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As per claim 5, Nakhimovsky and Rishi disclose the method of claim 1, Nakhimovsky further discloses the method comprising:  
freeing the second portion of the local memory in accordance with another programming statement that symbolically references the buffer name (Col 4, Lines 60-65).

As per claim 6, Nakhimovsky and Rishi disclose the method of claim 1, Nakhimovsky further discloses the method wherein the symbolic reference to the buffer name may be passed in at least one of: (i) a function, and (ii) a macro (Col 5, Line 44-45).

As per claim 7, Nakhimovsky and Rishi disclose the method of claim 1, Nakhimovsky further discloses the method comprising:  
translating the set of programming statements into code [all programming statements must be translated into code in order to be read by a computer (Col 2, Line 67 – Col 3, Line 1)]; and  
providing the code [The computer readable instructions are translated and then must be output somewhere, whether to storage or executed, thus they are provided].

As per claim 8, Nakhimovsky and Rishi disclose the method of claim 7, Nakhimovsky further discloses the method wherein the provided code is associated with at least one of: (i) assembly language, and (ii) microcode [The programming statements

of Nakhimovsky are created in C (Col 7, Line 26-31). All C code is translated into assembly language or microcode before it can be read by a computer].

As per claim 9, Nakhimovsky and Rishi disclose the method of claim 1, Nakhimovsky further discloses the method wherein the local memory comprises at least one of: (i) memory at the network processing element [The system memory is connected to the processors, which are interpreted as the network processing element in claim 1 (Fig 1, Ref 12 and 14)], (ii) hardware registers at the network processing element, and (iii) a local cache.

As per claim 14, please see rejection of claim 1 above. Claim 14 is rejected for similar reasons. [Note that Nakhimovsky discloses a storage medium having stored thereon instructions that when executed by a machine result in the method of claim 1 (Col 2, Line 63 – Col 3, Line 3)].

As per claim 15, Nakhimovsky and Rishi disclose the article of claim 14, Nakhimovsky further discloses the article wherein execution of the instructions further results in:

translating the set of programming statements into code [Programming statements must be translated into code for them to be understood by a computer, and therefore, to arrange the memory of claim 1 (Col 2, Line 67 – Col 3, Line 2)..

As per claim 16, Nakhimovsky and Rishi disclose the article of claim 15, Nakhimovsky further discloses the article wherein execution of the instructions further results in:

providing the code [The computer readable instructions are translated and then must be output somewhere, whether to storage or executed, thus they are provided].

As per claim 17, please see rejection of claim 14 above. Claim 17 is rejected for similar reasons.

As per claim 18, Nakhimovsky and Rishi disclose the article of claim 17, Nakhimovsky further discloses the article where said programming statements include: a programming statement that uses the buffer name to symbolically reference information that the second thread context will no longer store in the local memory at the network processing element (Col 4, Lines 60-65).

As per claim 19, Nakhimovsky discloses a method, comprising:  
defining a programming statement that is associated with a first thread (Col 3, Lines 1-4). Nakhimovsky does not disclose that the programming statement includes an indication of a read/write status. Rishi discloses a routine library having an indication of a read/write status associated with each allocation [A routine includes programming statements associated with memory allocated to a thread (Col 13 Lines 48-55; Col 14, Lines 1-11)]. Nakhimovsky further discloses the method wherein the programming

statement uses a buffer name to symbolically reference information that a first thread context will store in local memory at a multithreaded network processing element [Nakhimovsky discloses memory pools being numbered, since each memory pool contains a buffer, the buffers are also numbered. Thus, the data in the memory is symbolically represented by the number (name) of the buffer (Col 5, Lines 54-55)]; and defining a programming statement ~~that is~~ associated with a second thread (Col 3, Lines 1-4). Nakhimovsky does not disclose that the programming statement includes an indication of a read/write status. Rishi discloses a routine library having an indication of a read/write status associated with each allocation [A routine includes programming statements associated with memory allocated to a thread (Col 13 Lines 48-55; Col 14, Lines 1-11)]. Nakhimovsky further discloses the method wherein the programming statement uses the buffer name to symbolically reference information that a second thread context will store in local memory at the network processing element; [Nakhimovsky discloses memory pools being numbered, since each memory pool contains a buffer, the buffers are also numbered. Thus, the data in the memory is symbolically represented by the number (name) of the buffer (Col 5, Lines 54-55)]; wherein the symbolically referenced buffer name includes both letters and numbers [It would be obvious to use a name having both letters and numbers instead of just numbers to make identification of a thread easier. Furthermore, using numbers of Nakhimovsky is equivalent to the claimed letters and numbers since the computer system converts all letters and numbers to binary code, thus the representation is equivalent].

As per claim 20, Nakhimovsky and Rishi disclose the method of claim 19, Nakhimovsky further discloses the method comprising:

arranging for the programming statements to be translated into code

[Programming statements must be translated into code for them to be understood by a computer, and therefore, to arrange the memory of claim 1 (Col 2, Line 67 – Col 3, Line 2)].

As per claim 21, Nakhimovsky discloses a system, comprising:

a processor [Nakhimovsky discloses that the invention is a computer-readable medium. It is inherent that a computer has a processor); and a hard disk drive having stored therein instructions that when executed by a machine (Col 2, Lines 63-64) result in the following:

translating C programming language instructions into code [C Programming instructions must be translated into code for them to be understood by a computer, and therefore, to arrange the memory of claim 1 (Col 2, Line 67 – Col 3, Line 2)], and

Nakhimovsky does not disclose translating an additional programming statement into code, the additional programming statement including an indication of a read/write status. Rishi discloses a routine library having an indication of a read/write status associated with each allocation [A routine includes programming statements associated with memory allocated to a thread (Col 13 Lines 48-55; Col 14, Lines 1-11)].

Nakhimovsky further discloses using a buffer name to symbolically reference

information that a thread context will store in local memory at a multithreaded network processing element, [Nakhimovsky discloses memory pools being numbered, since each memory pool contains a buffer, the buffers are also numbered. Thus, the data in the memory is symbolically represented by the number (name) of the buffer (Col 5, Lines 54-55)].

wherein the symbolically referenced buffer name includes both letters and numbers [It would be obvious to use a name having both letters and numbers instead of just numbers to make identification of a thread easier. Furthermore, using numbers of Nakhimovsky is equivalent to the claimed letters and numbers since the computer system converts all letters and numbers to binary code, thus the representation is equivalent].

As per claim 22, Nakhimovsky and Rishi disclose the system of claim 21, Nakhimovsky further discloses the system comprising:

an interface to facilitate a transfer of the code from the system to the network processing element [It is inherent that an interface exist to facilitate transfer of the code from the system to the network processing element, as otherwise the units could not communicate. If the units are the same, they are interfaced as well.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the programming statements indicating read/write status, base, size and offset of Rishi into the system of Nakhimovsky, since Nakhimovsky and Rishi form the same field of endeavor, namely memory allocation and

this would allow for monitoring of the execution of the malloc command on Nakhimovsky and to track of access rights (Rishi, Col 13, Lines 48-52 and Col 14, Lines 4-6).

8. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakhimovsky in view of Rishi as applied to claim 1 above, and further in view of Liljeqvist.

As per claim 10, Nakhimovsky and Rishi disclose the method of claim 1. Nakhimovsky and Rishi do not disclose the method wherein the network processing element is a reduced instruction set computer microengine in a network device.

Liljeqvist discloses that a network processing element is a reduced instruction set computer microengine in a network device (The Processing Element, 1<sup>st</sup> Paragraph).

As per claim 11, the combination of Nakhimovsky, Rishi and Liljeqvist disclose the method of claim 10. Liljeqvist further discloses the method wherein the network device is associated with at least one of: (i) information packet header parsing, (ii) exception packet identification, (iii) information packet receipt, (iv) information packet transformation, and (v) information packet transmission (The Technological Incentive, 2<sup>nd</sup> Paragraph).

As per claim 12, the combination of Nakhimovsky, Rishi and Liljeqvist disclose the method of claim 10. Liljeqvist further discloses the method wherein the network

device is associated with at least one of: (i) Internet protocol information packets, (ii) Ethernet information packets, (iii) asynchronous transfer mode protocol, (iv) a local area network, (v) a wide area network, (vi) a network processor, (vii) a switch, and (viii) a router (The Technological Incentive, 2<sup>nd</sup> Paragraph; The Economical Incentive, 2<sup>nd</sup> Paragraph).

As per claim 13, Nakhimovsky, Rishi and Liljeqvist disclose the method of claim 12. Nakhimovsky further discloses the method wherein the set of programming statements includes at least one of: (i) an allocate buffer instruction (Col 5, Lines 44-45), (ii) a bind buffer address instruction, (iii) an activate buffer instruction, (iv) a deactivate buffer instruction, and (v) a free buffer instruction (Col 4, Line 63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the Reduced instruction set computer microengine of Liljeqvist into the system of Nakhimovsky and Rishi, since Nakhimovsky, Rishi and Liljeqvist form the same field of endeavor, namely processing elements and this would provide for higher performance by maximizing utilization in performing networking tasks (PE Configurations).

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on Mon-Fri 8-430.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 3, 2006

  
Leonid Kravets  
Patent Examiner  
Art Unit 2189

  
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PRIMARY EXAMINER